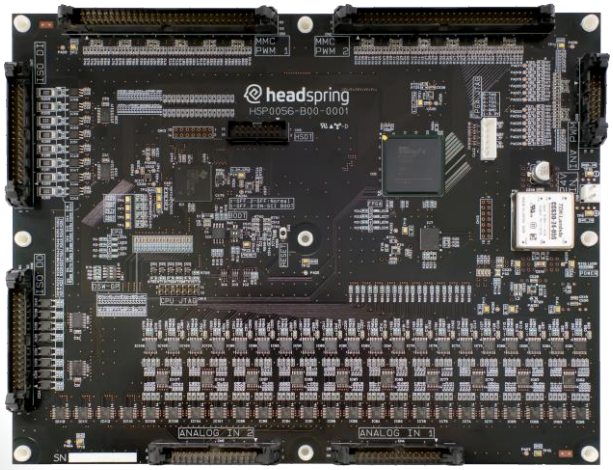
headspring
Sustainable Energy Solutions

Extended Controller for Power Electronics

HEC1-S1-B1



Power Electronics Controller with 108-gate / 40-channel AD Converter

Introduction

- Power Electronics Controller with 108 gate output ports and 40 channel of AD converter for Multi-level Inverter, Matrix Converter, Multi-axial Motor control system and many other solutions which require large number of gate channels
- Microcontroller from Texas Instruments “TMS320F28377S”, FPGA from Xilinx “XC6SLX75” on board. Microcontroller and FPGA are connected with 16-bit BUS to realize high speed control.
- Compatible with Headspring’s Power Electronics Development Toolset

Features

108 Gate Output, 40ch AD Input, Multi-purpose DIO

- ✓ Maximum of 48-phase of synchronized PWM output with dead-time can be generated
- ✓ 40ch of AD converter and simultaneous conversion of all the channel is possible
- ✓ Gate output ports and AD converters directly connected to FPGA
  ⇒Control system by FPGA is also available
- ✓ Multi-purpose DIO and LEDs are on board: Control of other systems is possible

FPGA Logic and Library Source Code Included

- ✓ Users can develop own logic by customizing the provided source code
- ✓ Customized FPGA logic can be supplied by Headspring as outsourcing

HSDT-DP, HSDT-GUI, HSLib Compatible

- ✓ Debug tools (real-time R/W of variables and oscilloscope function)
- ✓ Embedded libraries to utilize functions of microcontroller
- ✓ Debug with Step-execution and Break-point function using Texas Instruments’ Tool (CCS)

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Specification

Subject	Specification	Notes
Microcontroller	TMS320F28377S (Texas Instruments)	200MHz
FPGA	XC6SLX75 (Xilinx)	Spartan-6
Gate Output	96 port	(Negative Logic) 5V TTL
Gate Output for Inverter	12 port	(Negative Logic) 5V TTL
AD Input	40ch	0～5V, 2MS/s
Isolated Digital Input	16ch	24V
Isolated Digital Output	16ch	OC Output DC30V/50mA
Size	260mm×200mm	
Operational Temperature	0~50℃	No Condensation
Power Supply	DC24V±10%	
Power Consumption	< 30W	

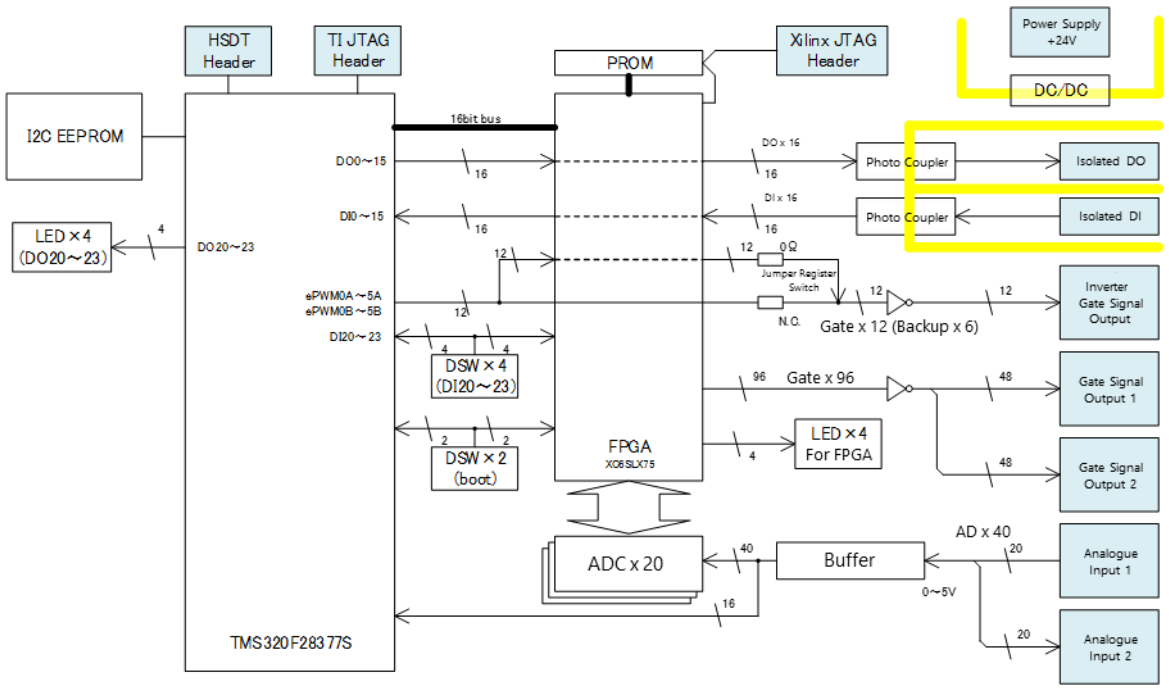
External I/F

Function	Description
Gate I/F	Gate Signal Output I/F from FPGA Total 96 ports from 2 connecter can be sent out.
Inverter I/F	Gate Signal Output I/F from Microcontroller. Two 3-phase inverter can be sent out.
HSDT I/F	Connection I/F for HSDT-DataProcessor For downloading Embedded Program, Debag using HSDT-GUI

Functions

Function	Description
Gate Signal Generation (96 port)	Gate Signal Generation by FPGA. 48-phase PWM Signal can be generated by standard FPGA Logic. Triangle waveform with phase shift for each channel is supported for Carrier Waveform
PWM Generation (12 port)	Synchronized PWM Generation Function. Triangle Waveform, Sawtooth Waveform, Reversed Sawtooth are supported for PWM Carrier Wave
AD Conversion (40ch)	14 bit AD Conversion connected to FPGA. Continuous conversion under standard FPGA Logic. Read function is available by using embedded software. Error function can be set by customizing Threshold.
AD Conversion (16ch)	12 bit AD Conversion by Microcomputer. Conversion Start Timing can be set by customizing PWM Generation Timer, Periodic Timer.
Digital I/O (16ch each)	Isolated Multi-purpose Digital I/O. R/W function by embedded library.
Multi-purpose LED Green: 4ch Red: 4ch	Operated by Embedded Program, FPGA. Connected to Microcontroller: 4ch Connected to FPGA: 4ch
Multi-purpose Dip Switch (4ch)	Read by Embedded Program, FPGA
EEPROM	Operated by Embedded Program. 512kbit by I2C connection

Block Diagram



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